Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A logic circuit diagram input device for estimating a layout area based on a logic circuit diagram constituted by transistors ~~a transistor~~ as a minimum unit, comprising:

hierarchy developing means for developing logic circuit diagram information having a hierarchical structure to information at a transistor level;

configuration parameter information extracting means for extracting configuration parameter information ~~such as~~ including at least one of a gate length, a gate width, a drain region area and a source region area ~~which are~~, the information being added to each transistor as a property;

area calculating means for calculating each transistor area using a transistor area calculation formula for calculating a transistor area from the [[said]] configuration parameter information; and

layout area estimating means for estimating a layout area by adding all areas of the transistors together,

wherein each transistor area calculated by said area calculating means is corrected using an area possession ratio per predefined transistor.

2. (Cancelled)

3. (Currently Amended) A logic circuit diagram input device for estimating a layout area based on a logic circuit diagram constituted by a plurality of standard cells [[cell]], comprising:

hierarchy developing means for developing logic circuit diagram information having a hierarchical structure to information at a standard cell level;

~~an each~~ a standard cell area holding part for holding ~~each standard cell area according to an instance~~ standard cell areas for respective instances, the instances each indicating an arrangement condition of each standard cell;

area deriving means for deriving ~~said developed each standard cell area according to the instance of the cell based on data of~~ areas of the standard cells included in the information from said [[each]] standard cell area holding part according to the instances respectively corresponding to the standard cells; and

layout area estimating means for estimating the layout area by adding all of the areas of the standard cells.

4. (Original) A logic circuit diagram input device according to claim 3, wherein said each standard cell area is corrected using an area possession ratio defined for each kind of the standard cell.

5. (Currently Amended) A logic circuit diagram input device according to claim 3, comprising:

wiring information extracting means for extracting wiring information from said logic circuit diagram information having the hierarchical structure; and

probable wiring possession area value holding means for holding [[a]] probable values ~~value~~ of [[a]] wiring possession areas [[area]], which is defined according to a layout area and the number of cells, wherein the sum of the probable values of the wiring possession areas which were extracted from the probable wiring possession area value holding means per wiring is added to said layout area.

6. (Currently Amended) A logic circuit diagram input device according to claim 5, comprising:

each block area wiring capacity of holding part for holding a probable wiring capacity value defined according to a layout area and the number of cells; and

probable wiring capacity value extracting means for extracting a probable wiring capacity value from said each block area wiring capacity holding part per wiring.

7. (Currently Amended) A logic circuit diagram input device according to claim 6, wherein information of said probable wiring capacity value is added to wiring data on the logic circuit diagram constituted by a plurality of standard cell as a property or an element.

8. (Currently Amended) A logic circuit diagram input device according to claim 1, wherein further detailed physical information ~~such as~~ including at least one of a maximum gate width, a unit resistance value, and a unit capacity value ~~or the like~~ is added ~~other than~~, in addition to the configuration parameter ~~such as a gate length, a gate width, a drain region area and source region area which were added to a transistor element as a property~~.

9. (Currently Amended) A logic circuit diagram input device according to claim 1 ~~claim 2~~, wherein an area possession ratio is set on higher level of block in stead of [[an]] the area possession ratio set per transistor.

10. (Original) A logic circuit diagram input device according to claim 1, wherein each cell, a block area and the number of basic cells (BC) which were estimated by the device are provided to a layout designing apparatus as an input file.

11. (Original) A logic circuit diagram input device according to claim 1, wherein each cell, a block area and the number of basic cells (BC) which were estimated by the device are stored in each instance element on a logic circuit diagram as a property.